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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,823	05/21/2004	Satoshi Tamura	60188-861	8403

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EXAMINER	
REAMES, MATTHEW L	
ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/849,823	TAMURA ET AL.	
	Examiner	Art Unit	
	Matthew L. Reames	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-5,13 are rejected under 35 U.S.C. 102() as anticipated by Lee (US 20030189215).

a. As to claim 1, Lee teaches a method for fabricating semiconductor devices, the method comprising the steps of: forming a semiconductor layer containing a positive layer (fig. 3 item 128) on a mother substrate (fig. 3 item 122); forming a metal layer on the semiconductor layer (fig. 7 item 156); separating the mother substrate from the semiconductor layer after forming the metal layer (fig. 8 and fig. 9); and removing a desired region of the metal layer from an exposed surface of the semiconductor layer from which the mother substrate has been separated to form a plurality of mutually separated semiconductor devices each containing the semiconductor layer (fig. 15 paragraph 49).

b. As to claim 2, Lee further teaches wherein the metal layer is composed of Au, Ag, or Cu (paragraph 19).

c. As to claim 3, Lee further teaches where the metal layer is formed by plating (paragraph 19).

d. As to claim 4, Lee teaches wherein the metal layer has a film thickness of 50 μm (paragraph 41).

e. As to claim 5, Lee teaches a step where separating the mother substrate is performed by irradiating a side of the semiconductor layer formed with the mother substrate with a laser (paragraph 42-43).

f. As to claim 7, Lee further teaches a step further comprising, between the step of forming the semiconductor layer and the step of separating the mother substrate, the step of: partly removing the semiconductor layer from a side of the semiconductor layer opposite to the side thereof formed with the other substrate to separate the semiconductor layer into a plurality of regions, wherein the plurality of semiconductor devices contain the plurality of respective regions (figure 3 and 4).

g. As to claim 13, Lee teaches a GaN layer (a group III nitride) (figure 3 item 128).

h. As to claim 14, Lee teaches a step after separating the mother substrate and before removing the desired metal layer: forming a passivation layer on the semiconductor layer (see eg. fig. 13 item 162).

2. Claims 1-5, and 12-13, are rejected under 35 U.S.C. 102(e) as being anticipated by Yoo (20040245543).

a. As to claim 1, Yoo teaches the processing step of forming a semiconductor layer on a substrate with a p-type layer (see fig. 9). Moreover Yoo teaches forming a metal layer on the semiconductor layer (see fig. 9 items 120-126). Yo teaches removing the substrate (see fig. 10) Yoo further teaches removing the metal layer layer from the exposed surface of the substrate (see fig. 11).

b. As to claim 2, Yoo further teaches, Au and Cu, see (fig. 9)

c. As to claim 3, Yoo further teaches plating (see abstract).

d. As to claim 4, Yoo teaches at 100 microns (see paragraph 80).

e. As to claim 5, Yoo teaches a laser lift off (see abstract)

f. As to claim 12, Yoo teaches cleaving by forming trenches (see fig. 11).

g. As to claim 13, Yoo teaches GaN (see abstract).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee.

a. As to claim 6,Lee does not explicitly teach a step where of separating the mother substrate is performed by polishing.

However it would have been obvious to one of ordinary skill in the art to have polished said structure/device to remove the "mother substrate."

One would have been so motivated since polishing can done at a much lower cost compared to similar method of removing the "mother substrate."

6. Claims 8-11 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Wong (US 6071795).

a. As to claims 8 and 9, Lee teaches the method as disclosed. However Lee does not teach further comprising, between the step of forming the metal layer and the step of forming the plurality of semiconductor devices, the step of: forming a polymer material film having an adhesive property on a surface of the metal layer opposite to a surface thereof formed with the semiconductor layer.

Wong teaches a step where the metal layer is bonded to an adhesive elastomeric (stretchable) film (a polymer) (column 6 lines 38-41 also fig. 9 and 10).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have applied the elastormeric substrate of Wong to the bottom of the device of Lee (the metal layer).

One would have been so motivated in order to have allowed easier transportation of a bulk number of devices described in Lee.

b. As to claims 10 and 11, Lee teaches the method as disclosed. However Lee does not teach a step further comprising, between the step of forming the metal layer and the step of separating the mother substrate, the step of: forming a semiconductor substrate having a cleaving property on a surface of the metal layer opposite to a surface thereof formed with the semiconductor layer.

However Wong teaches the use of a silicon substrate (a semiconductor) (fig. 3 item 110) underneath the metal layer (fig. 3 item 108).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have bonded a Si substrate to the metal layer of Lee.

One would have been so motivated in order to have increased the thermal conductivity of said device of Lee.

7. Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Wong.

b. Lee and Wong teach the method described in claim 10. Lee teaches an

etching to etch through the metal layer, and Wong teaches a cleave step to singulate the Si substrate (Abstract). Neither Lee nor Wong teach a step of forming the plurality of semiconductor devices includes the steps of: forming a trenched portion in a surface of the semiconductor substrate which has been exposed by removing the desired region of the metal layer; and cleaving the semiconductor substrate formed with the trenched portion to form the plurality of semiconductor devices.

However it would have been obvious to one of ordinary skill in the art at the time of the invention to use the method above to singulate the device of Lee/Wong.

One would have been so motivated since it was a standard technique for dicing/singulating semiconductor devices on a Si substrate, like that of Lee/Wong, at the time of the invention, and thus would have provided a cost benefit to the method.

Response to Arguments

8. The rejection Lee as a 102(b) has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Lee as a 102(e).

Applicant's arguments filed 4/7/2006 have been fully considered but they are not persuasive. This is taught by Lee since claim 1 recites "removing a desired region of the metal layer from an exposed surface of the semiconductor layer..." In this case the metal is removed from the semiconductor layer 128. The

semiconductor has a surface exposed to the metal layer and the p-contact, and that is the surface that it the metal is removed from. Applicant does not clearly indicate what the semiconductor layer is exposed to.

Moreover, if one is to interpret claim 1 so narrowly as to imply that that the removal process must be done from the exposed surface. Lee still teaches the step, since during the HCl step in fig. 11 some metal will inherently be removed in the process. Further this process is one of the steps required by Lee to separate the devices.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew L. Reames whose telephone number is (571)272-2408. The examiner can normally be reached on M-Th 6:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MLR

David Zarneke
Primary Exr
5/1/06